Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-10 (cancelled)

Claim 11 (previously presented) A method of storing a texel in a texel cache comprising:

reading a t coordinate of the texel, the t coordinate comprising a plurality of bits;

reading a s coordinate of the texel, the s coordinate comprising a plurality of bits; and

forming an offset by concatenating bits of the t coordinate with bits of the s coordinate,

wherein the texel is associated with a texture having a texture identification comprising a plurality of bits, further comprising forming an index signal by concatenating middle order bits of the s coordinate, middle order bits of the t coordinate, and at least one bit of the texture identification.

Claim 12 (previously presented) A method of storing a texel in a texel cache comprising:

reading a t coordinate of the texel, the t coordinate comprising a plurality of bits;

reading a s coordinate of the texel, the s coordinate comprising a plurality of bits; and

forming an offset by concatenating bits of the t coordinate with bits of the s coordinate,

wherein the texel is associated with a texture having an r coordinate comprising at least one bit, further comprising forming an index signal by concatenating middle order bits of the s coordinate, middle order bits of the t coordinate, and at least one bit of the r coordinate.

Claim 13 (previously presented) A method of storing a texel in a texel cache comprising:

reading a t coordinate of the texel, the t coordinate comprising a plurality of bits;

reading a s coordinate of the texel, the s coordinate comprising a plurality of bits; and

forming an offset by concatenating bits of the t coordinate with bits of the s coordinate,

wherein the texel has a main memory address comprising a plurality of bits, further comprising forming an index signal by concatenating middle order bits of the s coordinate, middle order bits of the t coordinate, and at least one bit of the main memory address.

Claim 14 (previously presented) An integrated circuit comprising:

a texture cache subsystem for storing a texel;

a cache address generator subsystem configured to provide an index and offset to the texture cache subsystem; and

a graphics pipeline subsystem configured to provide an s coordinate, a t coordinate, and a memory address to the cache address generator subsystem, and further configured to receive the texel from the texture cache subsystem,

wherein the index comprises bits of the s and t coordinates and at a least one bit selected from the group consisting of a texture id, a memory address, and an r coordinate.

Claims 15-37 (cancelled)

Claim 38 (previously presented) The method of claim 11 wherein the forming an offset by concatenating bits of the t coordinate with bits of the s coordinate is done by concatenating lower order bits of the t coordinate with lower order bits of the s coordinate.

Claim 39 (previously presented) The method of claim 38 further comprising storing the texel in a texel cache comprising a plurality of cache lines, wherein each cache line comprises a plurality of storage elements.

Claim 40 (previously presented) The method of claim 39 further comprising storing the texel in a storage element identified by the offset, the storage element in a cache line, the cache line identified by the index.

Claim 41 (previously presented) The method of claim 40 further comprising retrieving the texel from a main memory, wherein the texel has an address in main memory.

Claim 42 (previously presented) The method of claim 41 further comprising forming a tag by concatenating high order bits of the s coordinate with high order bits of the t coordinate and the address in main memory, and storing the tag in a look-up table.

Claim 43 (previously presented) The method of claim 12 wherein the forming an offset by concatenating bits of the t coordinate with bits of the s coordinate is done by concatenating lower order bits of the t coordinate with lower order bits of the s coordinate.

Claim 44 (previously presented) The method of claim 43 further comprising storing the texel in a texel cache comprising a plurality of cache lines, wherein each cache line comprises a plurality of storage elements.

Claim 45 (previously presented) The method of claim 44 further comprising storing the texel in a storage element identified by the offset, the storage element in a cache line, the cache line identified by the index.

Claim 46 (previously presented) The method of claim 45 further comprising retrieving the texel from a main memory, wherein the texel has an address in main memory.

Claim 47 (previously presented) The method of claim 46 further comprising forming a tag by concatenating high order bits of the s coordinate with high order bits of the t coordinate and the address in main memory, and storing the tag in a look-up table.

Claim 48 (previously presented) The method of claim 13 wherein the forming an offset by concatenating bits of the t coordinate with bits of the s coordinate is done by concatenating lower order bits of the t coordinate with lower order bits of the s coordinate.

Claim 49 (previously presented) The method of claim 48 further comprising storing the texel in a texel cache comprising a plurality of cache lines, wherein each cache line comprises a plurality of storage elements.

Claim 50 (previously presented) The method of claim 49 further comprising storing the texel in a storage element identified by the offset, the storage element in a cache line, the cache line identified by the index.

Claim 51 (previously presented) The method of claim 50 further comprising retrieving the texel from a main memory, wherein the texel has an address in main memory.

Claim 52 (previously presented) The method of claim 51 further comprising forming a tag by concatenating high order bits of the s coordinate with high order bits of the t coordinate and the address in main memory, and storing the tag in a look-up table.

Claim 53 (previously presented) The integrated circuit of claim 14 wherein the texture cache subsystem further comprises a texture cache for storing the texel, the texture cache arranged in cache lines, each cache line comprising a storage element.

Claim 54 (previously presented) The integrated circuit of claim 53 wherein the texel is stored in the texture cache in a storage element identified by the offset, the storage element in a cache line, the cache line identified by the index.

Claim 55 (previously presented) The integrated circuit of claim 54 further comprising a memory controller coupled to the texture cache subsystem, the memory controller configured to receive and provide texels from and to an external memory.

Claim 56-57 (cancelled)

Claim 58 (currently amended) ~~The graphics processor of claim 56~~ A graphics processor comprising:

a texture cache manager, coupled to receive texel addresses and provide packets of data and fetch requests;

a memory controller coupled to receive the fetch requests from the texture cache manager and provide cache line updates;

a FIFO coupled to receive the packets of data from the texture cache manager, where the FIFO stores the packets of data for a plurality of clock cycles; and

a texture cache controller coupled to receive the cache line updates from the memory controller and packets of data from the FIFO,

wherein the packets of data each comprise an offset of a first texel, an index of a first texel, and information required to generate an offset and an index of a second texel; and

wherein the index of the first texel ~~comprises at least a~~ is formed by concatenating middle order bits of an s coordinate of the first texel, middle order bits of a t coordinate of the first texel, and at least one bit of a texture identification associated with the first texel.

Claim 59 (currently amended) ~~The graphics processor of claim 56~~ A graphics processor comprising:

a texture cache manager, coupled to receive texel addresses and provide packets of data and fetch requests;

a memory controller coupled to receive the fetch requests from the texture cache manager and provide cache line updates;

a FIFO coupled to receive the packets of data from the texture cache manager, where the FIFO stores the packets of data for a plurality of clock cycles; and

a texture cache controller coupled to receive the cache line updates from the memory controller and packets of data from the FIFO,

wherein the packets of data each comprise an offset of a first texel, an index of a first texel, and information required to generate an offset and an index of a second texel; and

wherein the index of the first texel ~~comprises at least~~ is formed by concatenating middle order bits of an s coordinate of the first texel, middle order bits of a t coordinate of the first texel, and at least one bit of an r coordinate associated with the first texel.

Claim 60 (currently amended) ~~The graphics processor of claim 56~~ A graphics processor comprising:

a texture cache manager, coupled to receive texel addresses and provide packets of data and fetch requests;

a memory controller coupled to receive the fetch requests from the texture cache manager and provide cache line updates;

a FIFO coupled to receive the packets of data from the texture cache manager, where the FIFO stores the packets of data for a plurality of clock cycles; and

a texture cache controller coupled to receive the cache line updates from the memory controller and packets of data from the FIFO,

wherein the packets of data each comprise an offset of a first texel, an index of a first texel, and information required to generate an offset and an index of a second texel; and

wherein the index of the first texel ~~comprises at least a~~ is formed by concatenating middle order bits of an s coordinate of the first texel, middle order bits of a t coordinate of the first texel, and at least one bit of a main memory address associated with the first texel.